Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims:

1-6 (cancelled).

7 (currently amended): A method for simulating a switch used to control operations of outputting a radio signal, the method comprising:

establishing a first equivalent circuit, the first equivalent circuit comprising:

an input port for inputting the radio signal;

an output port for outputting the radio signal;

a first block connected to the input port, the first block having a first intrinsic inductor and a first intrinsic resistor;

a second block connected to the output port, the second block having a second intrinsic inductor and a second intrinsic resistor;

a third block connected to the first block and the second block, the third block having a gate capacitor, a gate inductor, and a gate resistor;

a first gate-substrate capacitor connected to the first block and the third block;

a second gate-substrate capacitor connected to the second block and the third block; and

a fourth block connected to the first gate-substrate capacitor and the second gate-substrate capacitor in series, the fourth block having a substrate capacitor, a first substrate resistor, and two second substrate resistors; and

~~establishing a second equivalent circuit, the second equivalent circuit including the first equivalent circuit and comprising:~~

~~a first channel block connected to the first block, the third block, and the first gate-substrate capacitor, the first channel having a first channel inductor, a first channel capacitor, and a first channel resistor;~~

~~a second channel block connected to the first channel block and having a second channel inductor, a second channel capacitor, and a second channel resistor; and~~

~~a third channel block connected to the second channel block, the second block, the third block, and the second gate-substrate capacitor, the second channel block being connected in series with the first channel block and the third channel block, the third channel having a third channel inductor, a third channel capacitor, and a third channel resistor;~~

utilizing the first equivalent circuit to simulate the switch at a turned-off state, ~~; and~~

~~utilizing the second equivalent circuit to simulate the switch at a turned-on state.~~

8 (cancelled).

9 (original): The method circuit of claim 7 wherein the switch is a metal-oxide semiconductor (MOS) transistor.

10 (new): The method circuit of claim 7 further comprising:

establishing a second equivalent circuit, the second equivalent circuit including the first equivalent circuit and comprising:

a first channel block connected to the first block, the third block, and the first gate-substrate capacitor, the first channel having a first channel inductor, a first channel capacitor, and a first channel resistor;

a second channel block connected to the first channel block and having a second channel inductor, a second channel capacitor, and a second channel resistor; and

a third channel block connected to the second channel block, the second block, the third block, and the second gate-substrate capacitor, the second channel block being connected in series with the first channel block and the third channel block, the third channel having a third channel inductor, a third channel capacitor, and a third channel resistor; and

utilizing the second equivalent circuit to simulate the switch at a turned-on state.

11 (new): The method of claim 10 wherein the first intrinsic resistor is connected to the first intrinsic inductor in series, the second intrinsic resistor is connected to the second intrinsic inductor in series, the gate resistor is connected to the gate inductor in series and connected to the gate capacitor in parallel, and the substrate capacitor is connected to the first substrate resistor in series and connected to the two second substrate resistors.

12 (new): The method of claim 11 wherein the first channel inductor is connected to the first channel capacitor in series and connected to the first channel resistor in parallel, the second channel inductor is connected to the second channel capacitor in series and connected to the second channel resistor in parallel, and the third channel inductor is connected to the third channel capacitor in series and connected to the third channel resistor in parallel.